IN THE CLAIMS

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims in accordance with the following:

1-13. (CANCELLED)

14. (currently amended) An interrupt control apparatus applied to a data processing system having a function of executing a conditional instruction that executes a designated data processing when a designated branch condition of the conditional instruction is satisfied, wherein a determination of the branch condition of the conditional instruction and the executed data processing when the branch condition of the conditional instruction is satisfied are indivisible, said apparatus comprising:

a break detection section for detecting a breakpoint set at an arbitrary position of an instruction sequence;

a condition determination section for determining whether an instruction of a designated address as an instruction located at an address specified as a break point address is executed as satisfying a branch condition of said conditional instruction; and

a control section for controlling a break-interrupt based upon a breakpoint detection result from said break detection section and execution of the instruction of the designated address according to a branch condition determination result from said condition determination section.

15. (currently amended) An interrupt control apparatus applied to a data processing system having a function of executing a conditional instruction that executes a designated data processing when a designated branch condition of the conditional instruction is satisfied, wherein a determination of the branch condition of the conditional instruction and the executed data processing when the branch condition of the conditional instruction is satisfied are indivisible, said apparatus comprising:

an instruction break detection section for detecting an instruction break in accordance with whether an instruction corresponding to an instruction address representing a breakpoint, which is set in a register, is read, and outputting a detection signal representing a detection result;

a condition determination section for determining whether an instruction of a designated address as an instruction located at an address specified as a break point address is executed as satisfying a branch condition of the conditional instruction, and outputting a branch condition determination signal; and

a logical operation section for performing an AND operation to said detection signal output from said instruction break detection section and execution of the instruction of the designated address according to said branch condition determination signal output from said condition determination section, and sending a break-interrupt notification in accordance with the AND operation result.

16. (PREVIOUSLY PRESENTED) An apparatus according to claim 15, wherein

said condition determination section is designed to determine whether an instruction word is said conditional instruction, if said instruction word is said conditional instruction, determine whether the branch condition of the conditional instruction is satisfied, and output the branch condition determination signal, and

when an instruction word corresponding to the instruction address representing said breakpoint is an unconditional instruction or a conditional instruction having an unsatisfied branch condition, said logical operation section does not send the break-interrupt notification, and when said instruction word is the conditional instruction having a satisfied branch condition, said logical operation section sends said break-interrupt notification.

17. (PREVIOUSLY PRESENTED) An apparatus according to claim 15, wherein

said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said instruction break is satisfied, and the branch condition of said conditional instruction is satisfied, and a second mode in which said break-interrupt is generated when said generation condition of said instruction break is satisfied,

said condition determination section is designed to determine whether an instruction word is said conditional instruction, if said instruction word is said conditional instruction, determine whether the branch condition of the conditional instruction is satisfied, and output the branch condition determination signal, and

in said first mode, when an instruction word corresponding to the instruction address representing said breakpoint is an unconditional instruction or a conditional instruction having an unsatisfied branch condition, said logical operation section does not sends the break-interrupt notification, and when said instruction word is the conditional instruction having a satisfied branch condition, said logical operation section sends the break-interrupt notification, and in said second mode, when said instruction word is an instruction word corresponding to the instruction address representing said breakpoint, said logical operation section sends said break-interrupt notification.

18. (PREVIOUSLY PRESENTED) An apparatus according to claim 15, wherein

said condition determination section is designed to determine whether an instruction word is said conditional instruction, if said instruction word is said conditional instruction, determine whether the branch condition of the conditional instruction is satisfied, and output the branch condition determination signal, and

when an instruction word corresponding to the instruction address representing said breakpoint is a conditional instruction having an unsatisfied branch condition, said logical operation section does not send the break-interrupt notification, and when said instruction word is an unconditional instruction or the conditional instruction having a satisfied branch condition, said logical operation section sends said break-interrupt notification.

19. (PREVIOUSLY PRESENTED) An apparatus according to claim 15, wherein

said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said instruction break is satisfied, and the branch condition of said conditional instruction is satisfied, and a second mode in which said break-interrupt is generated when said generation condition of said instruction break is satisfied,

said condition determination section is designed to determine whether an instruction word is said conditional instruction, if said instruction word is said conditional instruction, determine whether the branch condition of the conditional instruction is satisfied, and output the branch condition determination signal, and

in said first mode, when an instruction word corresponding to the instruction address representing said breakpoint is a conditional instruction having an unsatisfied branch condition, said logical operation section does not send the break-interrupt notification, and when said instruction word is an unconditional instruction or the conditional instruction having a satisfied branch condition, said logical operation section sends the break-interrupt notification, and in said second mode, when said instruction word is an instruction word corresponding to the instruction address representing said breakpoint, said logical operation section sends said break-interrupt notification.

20. (PREVIOUSLY PRESENTED) An apparatus according to claim 15, wherein said data processing system comprises one of a scalar processor for performing one unit of processing in accordance with one instruction, a long instruction word processor for parallel executing short instructions forming a long instruction word, and a parallel processor for parallel executing at least one basic instruction forming a variable-length instruction word.

21. (currently amended) An interrupt control apparatus applied to a data processing system having a function of executing a conditional instruction that executes a designated data processing when a designated branch condition of the conditional instruction is satisfied, wherein a determination of the branch condition of the conditional instruction and the executed data processing when the branch condition is satisfied are indivisible, said apparatus comprising:

an instruction break detection section for detecting an instruction break in accordance with whether an instruction corresponding to an instruction address representing a breakpoint, which is set in a register, is read, and sending a break-interrupt notification in accordance with the detecting of the instruction break; and

a control section for, in an interrupt handler activated in accordance with said break-interrupt notification supplied from said instruction break detection section, determining whether an instruction of a designated address as instruction located at an address specified as a break point address is executed as satisfying a branch condition of said conditional instruction, and controlling break-interrupt processing in accordance with the determining of execution of the

instruction of the designated address as satisfying the branch condition of the conditional instruction.

22. (PREVIOUSLY PRESENTED) An apparatus according to claim 21, wherein said control section determines, in said interrupt handler, whether an instruction word as an instruction break target is said conditional instruction, and when said instruction word is said conditional instruction, determines whether the branch condition of said conditional instruction is satisfied, and when said instruction word as said instruction break target is an unconditional instruction or a conditional instruction having an unsatisfied branch condition, returns from said interrupt handler, and when said instruction word as said instruction break target is a conditional instruction having a satisfied branch condition, performs said break-interrupt processing.

23. (PREVIOUSLY PRESENTED) An apparatus according to claim 21, wherein

said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said instruction break is satisfied, and the condition of the branch of said conditional instruction is satisfied, and a second mode in which said break-interrupt is generated when said generation condition of said instruction break is satisfied, and

in said first mode, said control section determines, in said interrupt handler, whether an instruction word as an instruction break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether the condition of the branch of said conditional instruction is satisfied, when said instruction word as said instruction break target is an unconditional instruction or a conditional instruction having an unsatisfied branch condition, returns from said interrupt handler, and when said instruction word as said instruction break target is a conditional instruction having a satisfied branch condition, performs said break-interrupt processing, and in said second mode, said control section performs said break-interrupt processing when receiving said break-interrupt notification.

24. (PREVIOUSLY PRESENTED) An apparatus according to claim 21, wherein said control section determines, in said interrupt handler, whether an instruction word as an instruction break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether the condition of the branch of said conditional instruction is satisfied, when said instruction word as said instruction break target is a conditional instruction having an unsatisfied branch condition, returns from said interrupt handler, and when

said instruction word as said instruction break target is an unconditional instruction or a conditional instruction having a satisfied branch condition, performs said break-interrupt processing.

25. (PREVIOUSLY PRESENTED) An apparatus according to claim 21, wherein

said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said instruction break is satisfied, and the condition of the branch of said conditional instruction is satisfied, and a second mode in which said break-interrupt is generated when said generation condition of said instruction break is satisfied, and

in said first mode, said control section determines, in said interrupt handler, whether an instruction word as an instruction break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether the condition of the branch of said conditional instruction is satisfied, when said instruction word as said instruction break target is a conditional instruction having an unsatisfied branch condition, returns from said interrupt handler, and when said instruction word as said instruction break target is an unconditional instruction or a conditional instruction having a satisfied branch condition, performs said break-interrupt processing, and in said second mode, said control section performs said break-interrupt processing when receiving said break-interrupt notification.

26. (PREVIOUSLY PRESENTED) An apparatus according to claim 21, wherein said data processing system comprises one of a scalar processor for performing one unit of processing in accordance with one instruction, a long instruction word processor for parallel executing short instructions forming a long instruction word, and a parallel processor for parallel executing at least one basic instruction forming a variable-length instruction word.

27. (currently amended) An interrupt control apparatus applied to a data processing system having a function of executing a conditional instruction that executes a designated data processing when a designated branch condition of the conditional instruction is satisfied, wherein a determination of the branch condition of the conditional instruction and the executed data processing when the branch condition is satisfied are indivisible, said apparatus comprising:

a software break detection section for detecting a software break in accordance with whether a breakpoint instruction placed at an arbitrary position of an instruction sequence is

executed, and sending a break-interrupt notification in accordance with the detection of the software break; and

a control section for, in an interrupt handler activated in accordance with said break-interrupt notification supplied from said software break detection section, determining whether an instruction of a designated address as an instruction located at an address specified as a break point address is executed as satisfying a branch condition of said conditional instruction, and controlling break-interrupt processing in accordance with the determining of execution of the instruction of the designated address as satisfying the branch condition of the conditional instruction.

28. (PREVIOUSLY PRESENTED) An apparatus according to claim 27, wherein said control section determines, in said interrupt handler, whether an instruction word as a software break target is said conditional instruction, and when said instruction word is said conditional instruction, determines whether the branch condition of said conditional instruction is satisfied, and when said instruction word as said software break target is an unconditional instruction or a conditional instruction having an unsatisfied branch condition, returns from said interrupt handler, and when said instruction word as said software break target is a conditional instruction having a satisfied branch condition, performs said break-interrupt processing.

29. (PREVIOUSLY PRESENTED) An apparatus according to claim 27, wherein

said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said software break is satisfied, and the branch condition of said conditional instruction is satisfied, and a second mode in which said break-interrupt is generated when said generation condition of said software break is satisfied, and

in said first mode, said control section determines, in said interrupt handler, whether an instruction word as a software break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether the branch condition of said conditional instruction is satisfied, when said instruction word as said software break target is an unconditional instruction or a conditional instruction having an unsatisfied branch condition, returns from said interrupt handler, and when said instruction word as said software break target is a conditional instruction having a satisfied branch condition, performs said break-interrupt processing, and in said second mode, said control section performs said break-interrupt processing when receiving said break-interrupt notification.

30. (PREVIOUSLY PRESENTED) An apparatus according to claim 27, wherein

said control section determines, in said interrupt handler, whether an instruction word as a software break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether the branch condition of said conditional instruction is satisfied, when said instruction word as said software break target is a conditional instruction having an unsatisfied branch condition, returns from said interrupt handler, and when said instruction word as said software break target is an unconditional instruction or a conditional instruction having a satisfied branch condition, performs said break-interrupt processing.

31. (PREVIOUSLY PRESENTED) An apparatus according to claim 27, wherein

said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said software break is satisfied, and the branch condition of said conditional instruction is satisfied, and a second mode in which said break-interrupt is generating when said generation condition of said software break is satisfied, and

in said first mode, said control section determines, in said interrupt handler, whether an instruction word as a software break target is said conditional instruction, when said instruction word is said conditional instruction, determines whether the branch condition of said conditional instruction is satisfied, when said instruction word as said software break target is a conditional instruction having an unsatisfied branch condition, returns from said interrupt handler, and when said instruction word as said software break target is an unconditional instruction or a conditional instruction having a satisfied branch condition, performs said break-interrupt processing, and in said second mode, said control section performs said break-interrupt processing when receiving said break-interrupt notification.

32. (PREVIOUSLY PRESENTED) An apparatus according to claim 27, wherein said data processing system comprises one of a scalar processor for performing one unit of processing in accordance with one instruction, a long instruction word processor for parallel executing short instructions forming a long instruction word, and a parallel processor for parallel executing at least one basic instruction forming a variable-length instruction word.

33. (currently amended) An interrupt control method for controlling a break-interrupt in a data processing system having a function of executing a conditional instruction that executes a designated data processing when a designated branch condition of the conditional instruction is satisfied, wherein a determination of the branch condition of the conditional instruction and the executed data processing when the branch condition of the conditional instruction is satisfied are indivisible, said method comprising:

detecting a breakpoint set at an arbitrary position of an instruction sequence;

determining whether an instruction of a designated address as an instruction located at an address specified as a break point address is executed as satisfying a branch condition of said conditional instruction; and

controlling the break-interrupt based upon the detecting of said breakpoint and execution of the instruction of the designated address according to the determining of the branch condition of said conditional instruction.

34. (currently amended) An apparatus comprising:

a controller

detecting a breakpoint at an arbitrary position of an instruction sequence;

determining whether execution of an instruction of a designated address as an instruction located at an address specified as a break point address ~~as satisfying~~satisfies a branch of an instruction;

controlling a break-interrupt based upon the detecting the breakpoint and the execution of the instruction of the designated address by the determining of the branch of the instruction, according to a logical operation of a detection signal from said breakpoint detection and a branch condition determination signal from said branch condition determination of the instruction; and

sending a break-interrupt notification in accordance with the logical operation.